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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,819	02/24/2004	Hiroshi Matsushita	03180.0355	1147

22852 7590 08/08/2005

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EXAMINER	
BARBEE, MANUEL L	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,819	MATSUSHITA ET AL.	
	Examiner	Art Unit	
	Manuel L. Barbee	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-20* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/04, 11/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 2/17/04*.

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to because of the following informalities: In claim 6, line 3 of the claim, delete "methods of", and insert --methods for--. Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 19 and 20 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. Claims 19 and 20 are directed to a computer program product configured to be executed by a computer. Since a computer program is merely a set of instructions capable of being executed by a computer, without being embodied on the computer-readable medium needed to realize the computer program's functionality, the claims are nonstatutory functional descriptive material. (See MPEP 2106).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 6, 8-13, 15-17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu (US Patent No. 6,392,434) in view of Sheu et al. (US Patent No. 6,694,208).

With regard to acquiring pass/fail maps for wafers for a plurality of types of semiconductor devices that display failure chip areas based on results of a plurality of electrical tests performed on a plurality of chip areas, as shown in claims 1, 10 and 19, Chiu teaches performing a series of electrical tests on a set of wafers and generating a wafer map that for each type of test marks the chips that fail (col. 2, lines 30-65). With regard to assigning a plurality of subareas, as shown in claims 1, 10 and 19, Chiu teaches dividing the wafer into subregions (col. 2, lines 11-29). With regard to calculating a characteristic quantity, as shown in claims 1, 10 and 19, Chiu teaches calculating the defect density for each subregion (col. 3, lines 14-29). With regard to obtaining correlation coefficients between the characteristic quantities corresponding to the respective subareas of the wafers to classify clustering failure patterns of the failure chip areas into categories by comparing the correlation coefficients with a threshold value, as shown in claims 1, 10 and 19, Chiu teaches comparing the failure density of a particular subregion with the failure density of other subregions and determining how many subregions have a defect density that is higher than a golden wafer (col. 3, line 41 - col. 4, line 36). With regard to manufacturing wafers having a plurality of types of semiconductor devices, as shown in claim 10, Chiu teaches different types of chips (col. 2, lines 42, 43).

Chiu does not teach classifying the electrical tests into a plurality of analogous electrical tests with regard to analogous failures, as shown in claims 1, 10 and 19. Sheu et al. teach determining the failure mode with the highest percentage of instances (col. 2, lines 1-17; col. 2, line 40 - col. 4, line 55). Different failure modes correspond to different electrical tests. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wafer test method, as taught by Chiu, to include classifying by failure mode, as taught by Sheu et al, because then the user would have been able to prioritize the failure mode and adjust for the failure causing the highest loss (Sheu et al. col. 1, lines 63-67).

With regard to failure densities, as shown in claims 3, 13 and 20, Chiu teaches calculating defect density (col. 3, lines 14-29). With regard to determining the cause of the failure by use of test statistics, as shown in claims 4 and 15, Chiu teaches correlating defect density calculations along with manufacturing information to determine the cause of defects (col. 3, line 41 - col. 4, line 36). With regard to a subarea database to store a plurality of area dividing methods, as shown in claims 6 and 16, Chiu teaches that the wafer may be divided into subregions in a plurality of methods (col. 2, lines 11-29). With regard to dividing the areas using circles concentric with the center of the wafer or a plurality of lines drawn from the center of the wafer, as shown in claims 8 and 11 and each of the subareas including at least one chip, as shown in claims 9 and 12, Chiu teaches using five concentric regions and four radial lines each including at least one chip (col. 2, lines 11-29; Fig. 1).

5. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu in view of Sheu et al. as applied to claims 1 and 10 above, and further in view of Behkami et al. (US Patent No. 6,775,630).

Chiu and Sheu et al. teach all the limitations of claim 1 upon which claim 2 depends and claim 10 upon which claim 14 depends. Chiu and Sheu et al. do not teach not teach appending manufacturing records including manufacturing processes and manufacturing apparatuses to the semiconductor devices, as shown in claims 2 and 14. Behkami et al. teach storing wafer maps and manufacturing data including equipment and history together as wafer characteristic data (col. 4, lines 1-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wafer test combination, as taught by Chiu and Sheu et al., to include wafer characteristic data, as taught by Behkami et al., because then wafer manufacturing data would have been tracked sufficiently to allow more less failures and lower costs (Behkami et al. col. 1, lines 47-65).

6. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu in view of Sheu et al. as applied to claims 1, 4, 10 and 15 above, and further in view of Buckheit et al. (US Patent Application Publication 2003/0055592).

Chiu and Sheu et al. teach all the limitations of claims 1 and 4 upon which claim 5 depends and claims 10 and 15 upon which claim 18 depends. Chiu and Sheu et al. do not teach a chi-square test statistic, as shown in claims 5 and 18. Buckheit et al. teaches using a chi-square test to determine if there are repeated failure chips in an area of a wafer (pars. 47-52). It would have been obvious to one of ordinary skill in the

art at the time the invention was made to modify the wafer test combination, as taught by Chiu and Sheu et al., to include a chi-square test, as taught by Buckheit et al., because then errors would have been classified as systematic, random or repeated allowing the most effective corrective measures to be taken (Buckheit et al., par. 9).

Allowable Subject Matter

7. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Manuel L. Barbee whose telephone number is 571-272-2212. The examiner can normally be reached on Monday-Friday from 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mlb
July 26, 2005

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